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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,665	12/08/2000	Christian Summerer	99 P 7719 US 02	6093

25962 7590 07/29/2004

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
PHAN, THAI Q	
ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/733,665	SUMMERER, CHRISTIAN	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed on Apr. 21, 2004. Claims 4-17 are now pending in the Action.

Drawings

Formal drawings filed in this application are acceptable for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishi Patent no. 6,411,386 B1.

As per claim 4, Kenji discloses a system for detecting an alignment mark on a semiconductor body with feature limitations substantially similar to the claimed invention (Abstract, Fig. 1, and Summary of the Invention). According to Kenji, the aligning apparatus measures positions of wafer marks, such alignment mark comprising a pair of sets of parallel lines disposed on the semiconductor wafer (Fig. 2), the parallel lines in one of the sets being orthogonal to the parallel lines in the other one of the set, wherein

the parallel line sets are laterally spaced overlaying relationship in X-Y direction (Fig. 2). The apparatus includes:

an optical system (Fig. 1, col. 6, lines 28-50) for illuminating and scanning an illuminated alignment mark on the semiconductor surface (Figs. 1, 6, col. 7, lines 56-65, col. 8, lines 45-53, col. 10, lines 22-42, col. 11, lines 4-50), the alignment mark (24X and 24Y) on the wafer surface comprising a pair of orthogonal lines in X-Y direction and laterally displaced from the other for reflecting impinging light of the orthogonal lines of reticle R on the wafer marks (Figs. 1, 2, 6, col. 6, line 51 to col. 7, line 5, col. 8, lines 5-22, col. 8, lines 45-53, col. 10, lines 22-42, col. 11, lines 4-50, col. 17, lines 13-28, for example). In other words, this wafer mark with orthogonal and laterally spaced lines pattern is for reflecting impinging light beam of the orthogonal pattern reticle R (col. 8).

detector or sensor (Fig. 1, col. 7, lines 55-65, for example) for detecting laterally displaced beams of the reflected light. Such sensor has a CCD-type two-dimensional image device (col. 7, lines 55-65) for detecting reflected lights from orthogonal directions (Figs. 2, 6, col. 10, lines 22-42, col. 11, lines 4-50, col. 17, lines 13-28, for example).

Kenji discloses an optical scanning system for scanning (Fig. 1, col. 6, lines 28-50) illumination light reflected from alignment mark (col. 8). Thus, this alignment mark with feature as shown above is to reflect impinging light of lateral spaced and orthogonal lines as claimed (col. 8, reticle pattern of X-Y orthogonal lines). Nishi also discloses pairs of orthogonal lines on wafer marks to reflect impinging light from illumination image light source (col. 7, lines 56-65), and laterally displaced from the

other one of such pair (24X and 24Y) to provide a pair of orthogonal lines of reflected and laterally displaced impinging lights (Figs. 2, col. 8, lines 5-22, col. 10, lines 22-35, for example).

Kenji discloses a CCD-type detector for detecting reflected light beams from wafer mark but does not expressly disclose a pair of detectors spaced laterally to detect reflected lights as claimed.

It would have been obvious for practitioner in the art at the time of the invention was made to find Kenji detector having CCD-type two dimensional (array) image sensor implied the claimed limitation of pair of detectors spaced laterally because typical CCD-type two dimensional image sensor has an array of sensing elements, or at least a pair of sensors as claimed, arranged in two dimension usually lateral spacing, for detecting signals reflected from the illuminated wafer mark.

As per claims 5 and 6, Kenji discloses impinging light line or illumination beam is projected onto the wafer surface, particularly to the wafer mark area, in a X and Y direction (Figs. 2, 3). It would be obvious for skilled in the art to arrange the wafer mark and optical scanning beam in the claimed direction to detect wafer alignment.

As per claim 7, Kenji discloses the alignment light line of wafer mark (24X1, 24X2) are separated laterally along the X-axis by a distance W, for instance ((Figs. 2a and 2b).

As per claims 8-17, Kenji teaches alignment marks with features above would imply the claimed limitations to detect wafer mark alignment on the semiconductor body.

Response to Arguments

1. Applicant's arguments filed Apr. 21, 2004 have been fully considered but they are not persuasive.

2. In response to applicant's argument Nishi does not disclose or suggest "alignment mark comprising a pair of sets of parallel lines ... being in an overlaying relationship" (see page 5, paragraph 4), the examiner disagrees with this statement. It's because the argued feature of parallel lines ... being in an overlaying relationship does not appear in claim 4, particularly, in the claim functional embodiment for consideration.

3. In response to applicant's argument Nishi does not disclose an optical system for scanning an alignment illumination comprising a pair of orthogonal lines for impinging light over the surface of the alignment mark, one of such pair of impinging light lines being orthogonal to, and laterally displaced from, the other one of such pair of impinging light lines (page 5, last paragraph), the examiner disagrees with.

Kenji discloses an optical system (Fig. 1, col. 6, lines 28-50) for illuminating and scanning an illuminated alignment mark on the semiconductor surface (Figs. 1, 6, col. 7, lines 56-65, col. 8, lines 45-53, col. 10, lines 22-42, col. 11, lines 4-50), the alignment mark (24X and 24Y) on the wafer surface comprising a pair of orthogonal lines in X-Y direction and laterally displaced from the other for reflecting impinging light of the orthogonal lines of reticle R on the wafer marks (Figs. 1, 2, 6, col. 6, line 51 to col. 7, line 5, col. 8, lines 5-22, col. 8, lines 45-53, col. 10, lines 22-42, col. 11, lines 4-50, col. 17, lines 13-28, for example). In other words, this wafer mark with orthogonal and

laterally spaced lines pattern is for reflecting impinging light beam of the orthogonal pattern reticle R.

Kenji optical scanning system is for scanning (Fig. 1, col. 6, lines 28-50) illumination light reflected from alignment mark (col. 8). Thus, this alignment mark with feature as shown above is to reflect impinging light of lateral spaced and orthogonal lines as claimed (col. 8, reticle pattern of X-Y orthogonal lines). Nishi also discloses pairs of orthogonal lines on wafer marks to reflect impinging light from illumination image light source (col. 7, lines 56-65), and laterally displaced from the other one of such pair (24X and 24Y) to provide a pair of orthogonal lines of reflected and laterally displaced impinging lights (Figs. 2, col. 8, lines 5-22, col. 10, lines 22-35, for example).

4. In response to applicant's argument Kenji does not expressly disclose a pair of detectors spaced laterally to detect reflected lights as claimed, the examiner responds that Kenji discloses a CCD-type detector for detecting reflected light beams from wafer mark. It would have been obvious for practitioner in the art at the time of the invention was made to find Kenji detector having CCD-type two dimensional (array) image sensor implied the claimed limitation of pair of detectors spaced laterally because typical CCD-type two dimensional image sensor has an array of sensing elements, or at least a pair of sensors as claimed, arranged in two dimension usually in lateral spacing, for detecting signals reflected from the illuminated wafer mark.

5. In response to applicant's argument to the double patenting rejection in the last Office Action, and due to the present claimed application subjected to restriction before (see page 6, last paragraph and page 7, paragraph 1), the double patenting rejection has been withdrawn in this Action.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US patent no. US 6654097 B1, issued to Nishi, Kenji, on Nov. 2003

2. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 703-305-3812. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 20, 2004

Thai Phan

Thai Phan
Patent Examiner
Art Unit: 2128